Remarks/Argument

Objection to the Drawings

The drawings are amended to delete extraneous reference numbers 501, 503, 507, 508 and 509 in Figure 5 and relabel the inside circle of radius C in Figure 5B with the number 507 to correct the inadvertent use of the number 505 to designate two different features. Corresponding deletion of the unused reference numbers are made to Figure 6. Figure 9 is amended delete the unused reference numeral 910, while paragraph 0098 of the specification is amended to correct a typographical error by replacing the number 808 with the number 908 in connection with the description of the associated step depicted in Figure 9. The specification is further amended at paragraph 109 to correct the reference to step 1403 and to reference the "yes" outcome associated with the box 1405 of the drawings.

Objections to the Specification

The Abstract of the Disclosure is amended to comport with the maximum word length requirement. However, no correction is believed necessary or desirable in connection with the term "pairwise". Contrary to the Examiner's statement, as used in the specification, the term "pairwise" is properly a single word. It is noted that this term in the form of a single word is widely used throughout the art and related arts as evidenced by a search of issued U.S. Patents indicating that 4571 patents issued since 1976 use this term, 520 patents using it in one or more claims, while 2869 documents are found in a search of the PGPUB Production Database for Published U.S. Patent Applications using this term. For example, the Examiner's attention is directed to U.S. Patent No. 6,378,105 in which he is indicated to be the Assistant Examiner and in which the term "pairwise" is used as a single word. Numerous other example abound. Accordingly, no correction is believe necessary.

Amendment to the Claims

Independent claims 1, 8 and 15 are amended to particularly pint out and distinctly claim the subject matter which the Applicant regards as the invention by the addition of language requiring that the combinational logic be configured to combine pairs of index values to form corresponding pairwise combined hash indices. New claims 21, 23 and 25 dependent from

respective base claims 1, 8 and 15 further recite that the index values be combined in pairs that are in lexicographical order, while dependent claims 22, 24 and 26 require that the hash indices be formed by concatenating said index values in lexicographical order.

There being no prior art rejection of claims 13 and 14, each is rewritten in independent form including the subject matter of base claim 8 as originally presented. Accordingly, it is understood that these claims are considered to be patentably distinguishable over the art of record and are now considered to be *prima facie* in condition for allowance.

Rejection of Claims Under 35 USC §112 ¶1

The Examiner has taken the position that the specification fails to teach an inverse fault-tolerant decoder, a reverse perfect error correction code or a reverse Golay code and has accordingly rejected claims 1-7, 13 and 15-20. The rejection is respectfully traversed.

As an initial point, it is noted that the Applicant is entitled to be his own lexicographer where the terminology adopted is not contrary to accepted meanings. See MPEP §2173.01 *Claim Terminology* citing *In re Swinehart*, 439 F.2d 210, 160 USPQ 226 (CCPA 1971),(a claim may not be rejected solely because of the type of language used to define the subject matter for which patent protection is sought) and MPEP §2111.01 citing In re Hill, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). As described in Applicant's specification, a conventional error correction scheme uses an encoder to add some redundancy to data so that subsequent distortions of the resultant code can be detected and corrected. The redundancy is typically added by the addition of some number of bits. The expanded code word is then decoded to recover the original data, the redundant or error correction information being used to correct any distortions and then discarded, leaving only the original data. The present invention reverses this process by utilizing the decoding process on original data to obtain a hash index. That is, instead of adding redundancy to data, the present invention eliminates information distinguishing data from similar data. Accordingly, similar data produces one or more indices in common when processed according to known error detection and correction decoding schemes. So as to distinguish the use of the prior art decoding method for the purpose of restoring data from the present use to provide an index, Applicant has adopted the terminology "inverse fault tolerant decoder". The mere fact that Applicant has used slightly different terminology (i.e., "inverse fault tolerant

decoder") from that which the Examiner appears to find acceptable (i.e. "error-correction decoder") to distinguish the new use of an existing process does not render the specification non-enabling. At most, even if the terminology were confusing (which it certainly is not), the Examiner might object to the .

The Examiner rejection based on the terminology "a reverse perfect error correction code" similarly refers to the decoding process specified by an error correction code, in this case, a "perfect error correction code" Perfect codes and what make a code "perfect" are well known. See, for example, U.S. Patent No. 4,340,963 ("[i]f the error correcting code is not a perfect code, there will be some syndrome patterns which do not correspond to a pattern of up to t errors."); 4,414,667 ("[t]he Golay code is a perfect code in that each codeword differs from every other codeword by exactly seven bits, which difference represents the so-called Hamming distance."), 4,586,183 ("[f]or a so-called perfect code, an example of which is the single error correcting Hamming code, the number of addresses identifiable by the check words is equal to the number of addresses where an error may occur."); and 4,648;091("[t]he basic Golay (23,12) code words are the only known possible binary perfect code words with multiple-error correction capability.") Applicant's specification explains that "[t]he Hamming code (7,4,3) is perfect in the sense that the codewords represent all possible 7-bit combinations: 27 = 128." See paragraph [0015]. The use of the term "reverse" to emphasize that the present invention subjects data to the decoding process to obtain a hash code rather than to correct for distortions to the data does not amount to a lack of enablement.

For the reasons presented above, the rejection of claims under 35 USC §112, ¶1 is respectfully traversed and withdrawal thereof is requested.

Rejection of Claims Under 35 USC §112 ¶2.

The Examiner appears to have taken the position that the claims are fatally indefinite because the language "pairs of said index values" does not find support in the earlier recitation of "a plurality of predetermined index values". The former phrase refers to pairs of index values, the index values previously described as being a plurality and predetermined. The undersigned is unable to identify any indefiniteness in the language and therefore respectfully traverses the

rejection. However, if the Examiner has suggested language that he would prefer, he is encouraged to contact the undersigned to discuss the adoption of any proposed changes.

Rejection of Claims Under 35 USC §§102(b) and 103(a)

Claims 1-5 and 15-1 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Berkovich et al. (Berkovich, S., El-Qawasmeh, E., "Reversing the Error-Correction Scheme for a Fault-Tolerant Indexing", The Computer Journal, vol. 43, no. 1, pp. 54 - 64, January 2000).

35 U.S.C. 103(a) rejection of claims 1 and 15. According to the Examiner:

> *...Berkovich teaches that a data vector 1001 100 is transformed into 8 index values that are predetermined in the table of Figure 4 by adding the data vector 1001 100 to all vectors of weight 1); a computational arrangement to combine pairs of said index values to form corresponding, combined hash indices (a computational arrangement in Figure 4 of Berkovich is used to combine the 8 index values calculated by adding the data vector 1001 100 to all vectors of weight 1 to form the 4 corresponding, combined hash indices 101 1 , 0001, 1000 and 11 01...*

Office Action at Page 6.

Note only is the comparison technically inappropriate, but it fails to satisfy the literal language of the rejected claims. In particular, the cited portion of Berkovich describes making slight alterations to what the claims call a data vector by flipping one bit at a time to obtain all 1-bit distortions of the data vector. The data vector is then "hashed" to obtain an index value into a hash table. The "arrangement to combine pairs of said index values" asserted by the Examiner does not; it performs a mod 2 addition of a data vector with what amounts to a mask to produce respective 1-bit distortions. That is, the applied reference manipulates the data vector itself, not the indices produced by decoding the data vector according to an error-correction code. Neither is there a teaching to combine pairs of the resultant index values to form corresponding pairwise combined hash indices" (emphasis added).

The Examiner further takes the position that:

> *...Berkovich does not explicitly teach the specific use of **combinational logic** configured to combine pairs of said index values to form corresponding.*
> *The Examiner asserts that the operation of combining pairs of index values to form corresponding, combined hash indices is a binary operation hence it would be obvious to use combinational logic to*

> *combine pairs of said index values to form corresponding, combined hash indices based on obvious engineering design choices since that is what combinational logic is designed for.*
> *Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Berkovich by including use of* ***combinational logic*** *configured to combine pairs of said index values to form corresponding. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of* ***combinational logic*** *configured to combine pairs of said index values to form corresponding would provide the opportunity to implement the method taught in the Berkovich paper based on obvious engineering design choices using combinational logic since that is what combinational logic is designed for.*

Office Action at page 7 (emphasis in original).

Again, since Berkovich does not teach combining pairs of index values resulting from transformation of a data vector by an inverse fault-tolerant decoder, it is understandable that the reference also fails to describe or suggest use of combinational logic to combine the pairs. In any case, there mere assertion that using combinational logic is a mere design choice by "that is what combinational logic is designed for" is circular and, contrary to the Examiner's assertion, does not render the combination obvious pursuant to 35 U.S.C. §103(a).

For the reasons present, the rejection of claims 1 and 15 and respective dependent claims 2-4 and 16-18 is considered to be improper and withdrawal thereof is respectfully solicited.

Claims 8- stand rejected under 35 U.S.C. 102(b) as being anticipated by Berkovich. As in the rejection of claims 1 and 15, the Examiner again relies on Berkovich for teaching "a computational arrangement [as depicted] in Figure 4 of Berkovich [that] is used to combine the 8 index values calculated by adding the data vector 1001 100 to all vectors of weight 1 to form the 4 corresponding, combined hash indices 101 1,0001, 1000 and 1101..." in satisfaction of the requirement for combining pairs of index values to form corresponding combined hash indices. While it is believed that the original language of claim 8 was distinguishable as originally presented, the present amendment emphasizes that the step of combing pairs of the index values is effective "to form corresponding pairwise combined hash indices". Berkovich fails to describe of suggest such pairwise combined hash indices. These "pairwise" combined hash indices may be depicted as ordered pairs as shown in Figures 12B, 12B and 12D of the drawings; the indices

may be arranged in lexographical order as described at paragraph 40 of the specification, and may be a concatenation of the indices "to double the size of the hash key." Berkovich fails to describe or suggest such a combination of index values. Accordingly, claim 8 together with the claims dependent therefrom are each considered to be distinguishable over the applied prior art and withdrawal of the outstanding rejection of those claims is respectfully requested.

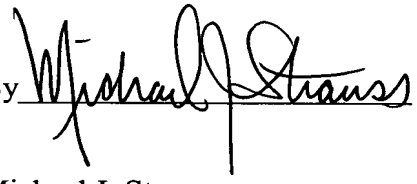
No art has been applied against claims 13 and 14, each of which has been rewritten in independent form including the limitations of base claim 8 as originally presented. Accordingly, these claim are also considered to be allowable.

In view of the foregoing, the application including claims 1-26 is now considered to be in condition for allowance and an early notification thereof is respectfully requested.

A check for the amount of $122.00 accompanies this Amendment in payment of the extra claim fee. If any additional fee is due, please charge our Deposit Account No. 06-2375, under Order No. 714.001/10108288 from which the undersigned is authorized to draw.

Dated: April 28, 2004

Respectfully submitted,

By 

Michael J. Strauss
Registration No.: 32,443
FULBRIGHT & JAWORSKI L.L.P.
Market Square
801 Pennsylvania Avenue, N.W.
Washington, DC 20004-2623
(202) 662-0200
(202) 662-4643 (Fax)
Attorney for Applicant

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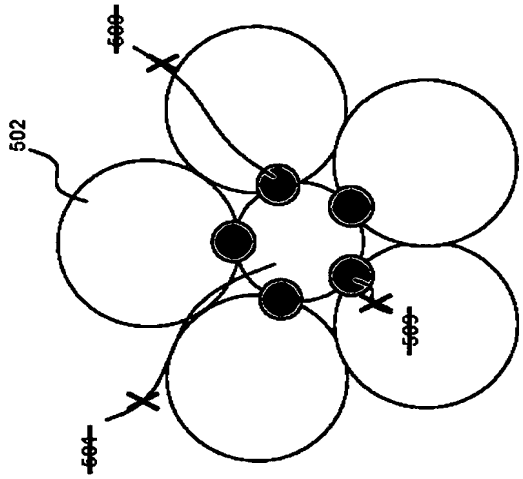

Figure 6B

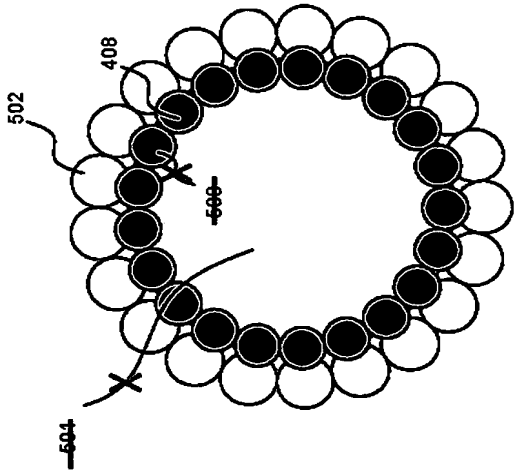

Figure 6A

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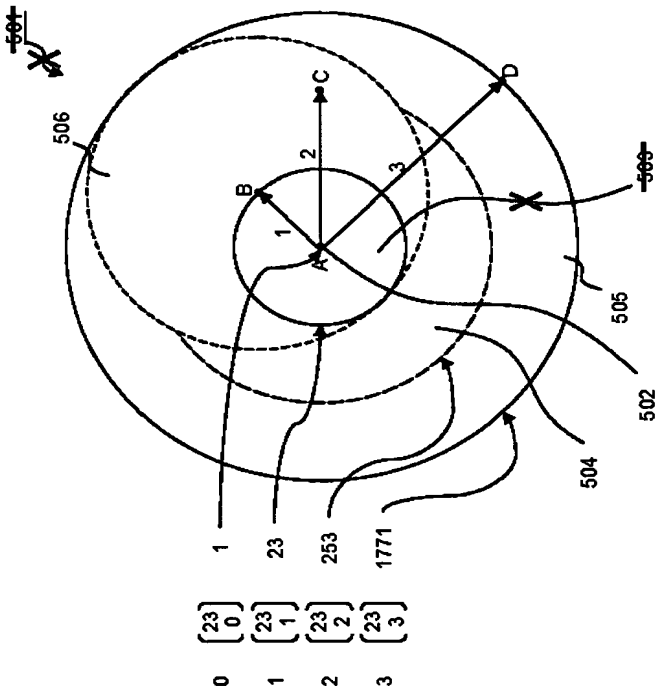

Figure 5A

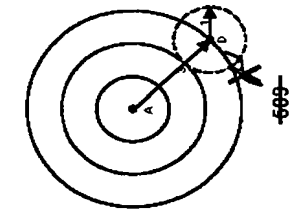

Figure 5E

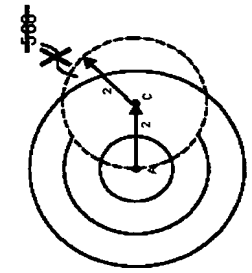

Figure 5D

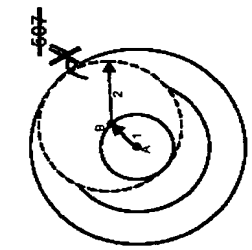

Figure 5C

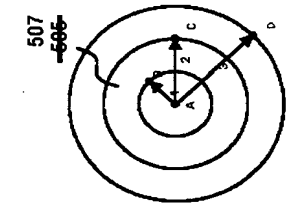

Figure 5B

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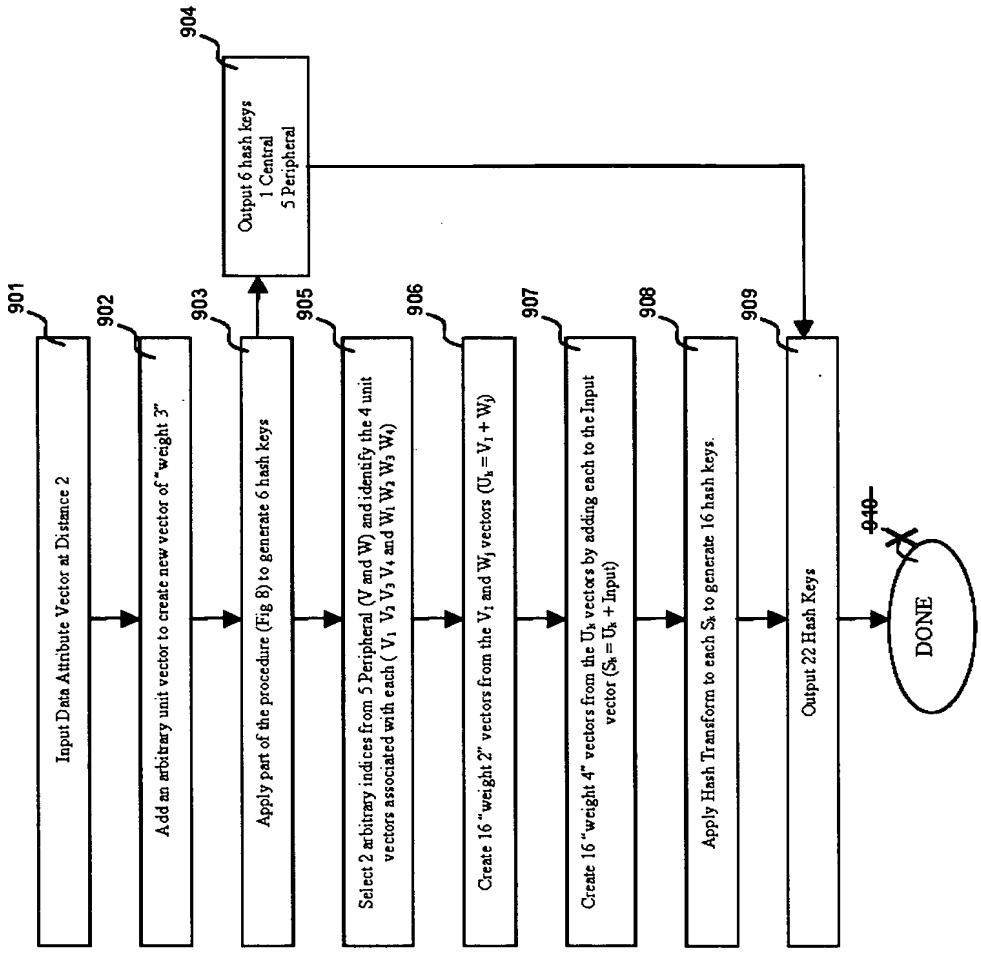

Figure 9